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10/643,665	08/19/2003	John Malvern Swope	200205326-1	5751

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,665	SWOPE, JOHN MALVERN	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/643,665 filed 08/19/2003.

2. Claims 1-22 are pending in the Application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

3. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. With respect to claims 1, 13 and 18, the omitted structural cooperative relationships are:

a) it is not clear what relationship between first and second limitation is, i.e. how generating of "low level details" in the second limitation (second sublimitation for claim the 13) related to "one or more low level details" of the first limitation (first sublimitation of the claim 13);

b) it is not clear what information or data was used in order to "determine one or more high level constraints" in the second limitation (second sublimitation for the claim 13);

c) it is not clear what kind of "information to generate the low level details" was used in the second limitation (second sublimitation for the claim 13): the information before or after compilation procedure;

d) it is not clear in the third limitation (third sublimitation for the claim 13) if "the printed circuit board design module includes the **information**" before or after compilation procedure;

e) it is not clear how "generating the printed circuit board design module" in the third limitation (third sublimitation for the claim 13) related to "the low level details" in the first and second limitations (second sublimitation for the claim 13).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al. (US Patent Application Publication 2005/0086626).

With respect to claims 1 and 18 Sato et al. teaches a method for generating a printed circuit board design module (paragraph [0003]); a computer-readable medium storing a printed circuit board design module executable by a computer system (paragraphs [0008], [0015], comprising: compiling information that is usable to derive one of more low level details associated with a printed circuit board as shown on the Fig. 3 wherein the information from general floor planner 1 and circuit editor 3 is compiled to derive one or more low level details associated with a printed circuit board

such as general layout & wiring and circuit information to feed advice engine group 24 (paragraphs [0010], [0091]); determining one or more high level constraints that are usable with the information to generate the low level details as shown on the Fig. 3 the advice engine group 24 as a result of feeding by the information of the general layout & wiring and circuit information determines design constraints which along with circuit editor 3 generate CIRCUIT INFO (low level details) (paragraph [0094]); and generating the printed circuit board design module such that the printed circuit board design module includes the information and such that the printed circuit board design module is configured to receive the one or more high level constraints within the mapping to layout & wiring editor as S21 shown on the Fig. 12, wherein the design constraints obtained from advice engine group 24 are combined with the information obtained from the circuit editor (paragraph [0011]) to generate the output layout and wiring information (paragraph [0013]), wherein the step S22 is for deciding whether or not the mapped result satisfies the layout and wiring constraints (paragraph [0012]).

With respect to claim 13 Sato et al. teaches a computer system within an electronic designing apparatus for designing electronic circuit (paragraph 0014]) comprising: a processor as shown on the Fig. 2 depicting the computer system 100 for implementing the electronic circuit design method (paragraph [0085]) including processor CPU 201; and a memory within memory section 202 as shown on the Fig. 2 (paragraphs [0088]) that includes a printed circuit board design module that is executable by the processor (paragraph [0087]), the printed circuit board design module being generated by: compiling information that is usable to derive one of more low level

details associated with a printed circuit board as shown on the Fig. 3 wherein the information from general floor planner 1 and circuit editor 3 is compiled to derive one or more low level details associated with a printed circuit board such as general layout & wiring and circuit information to feed advice engine group 24 (paragraphs [0010], [0091]); determining one or more high level constraints that are usable with the information to generate the low level details as shown on the Fig. 3 the advice engine group 24 as a result of feeding by the information of the general layout & wiring and circuit information determines design constraints which along with circuit editor 3 generate CIRCUIT INFO (low level details) (paragraph [0094]); and generating the printed circuit board design module such that the printed circuit board design module includes the information and such that the printed circuit board design module is configured to receive the one or more high level constraints within the mapping to layout & wiring editor as S21 shown on the Fig. 12, wherein the design constraints obtained from advice engine group 24 are combined with the information obtained from the circuit editor (paragraph [0011]) to generate the output layout and wiring information (paragraph [0013]), wherein the step S22 is for deciding whether or not the mapped result satisfies the layout and wiring constraints (paragraph [0012]).

With respect to claims 2-12, 14, 15, 19 and 20 Sato et al. teaches:

Claim 2: generating a list of the low level details prior to compiling the information within the general floor planner 1, which has an ability of inputting and outputting the general layout and wiring information (paragraph [0091]);

Claim 3: the high level constraints include schematic constraints as shown on the Fig. 8, wherein the design constraints are represented in the graphical (schematic) format (paragraph [0105]);

Claim 4: the high level constraints include electrical constraints within consideration of the electrical characteristics of the devices involved into circuit design during the implementation of the design constraints (paragraph [0143]), wherein electrical characteristics are included into the device specification (paragraph [0097]);

Claim 5: the high level constraints include mechanical constraints within the user resources 23 shown on the Fig. 3, which includes mechanical characteristics in the substrate specification, such as substrate technology, number of layers, layer structure etc. and feeds the advice engine group 24 for generating the design constrains (paragraph [0097]);

Claim 6: the high level constraints include cost constraints within the information including the cost contained in the device specification, wherein this information feeds the advice engine group 24 for generating the design constrains (paragraph [0097]);

Claim 7: the low level details include routing details within a **general** layout and wiring information related to devices and **wiring** (paragraph [0091]);

Claim 8: the low level details include component placement details within a **general** layout and wiring information related to **devices** and wiring (paragraph [0091]);

Claim 9: the low level details include stack-up details within substrate specifications including the substrate technology, wherein the information of the

substrate specification is fed into the advice engine group 24 for generating the design constrains (paragraph [0097]);

Claims 10, 14 and 19: the information includes mathematical equations usable to calculate the low level details using the high level constraints as shown on the Figs. 8-10, wherein the information of the general floor planner 1 (Fig. 3) is represented as mathematical expression (paragraph [0117]);

Claims 11, 15 and 20: the information includes a table usable to determine the low level details using the high level constraints as shown on the Fig. 9 the table including the low level details represented as mathematical expression of the design constraint (paragraph [0106]);

Claim 12: generating the printed circuit board design module such that the printed circuit board design module is configured to receive the one or more high level constraints from a user interface incorporated into a schematic software tool within the mapping to layout & wiring editor as S21 shown on the Fig. 12, wherein the design constraints obtained from advice engine group 24 are combined with the information obtained from the circuit editor (paragraph [0011]) to generate the output layout and wiring information (paragraph [0013]), wherein the step S22 is for deciding whether or not the mapped result satisfies the layout and wiring constraints (paragraph [0012]) ans as shown on the Fig. 13, wherein in the step S35the output is layout and wiring constraints, which are displayed on the display screen 102 a shown on the Fig. 1 of the display 102 shown on the Fig. 2 (paragraph [0120]).

With respect to claims 16, 17, 21 and 22 Sato et al. teaches:

Claims 16 and 21: the high level constraints are selected from the group consisting of schematic constraints as shown on the Fig. 8, wherein the design constraints are represented in the graphical (schematic) format (paragraph [0105]), electrical constraints within consideration of the electrical characteristics of the devices involved into circuit design during the implementation of the design constraints (paragraph [0143]), wherein electrical characteristics are included into the device specification (paragraph [0097]), and mechanical constraints within the user resources 23 shown on the Fig. 3, which includes mechanical characteristics in the substrate specification, such as substrate technology, number of layers, layer structure etc. and feeds the advice engine group 24 for generating the design constrains (paragraph [0097]);

Claim 17 and 22: the low level details are selected from the group consisting of routing details within a **general** layout and wiring information related to devices and **wiring** (paragraph [0091]), component placement details within a **general** layout and wiring information related to **devices** and wiring (paragraph [0091]), and stack up details within substrate specifications including the substrate technology, wherein the information of the substrate specification is fed into the advice engine group 24 for generating the design constrains (paragraph [0097]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800